Stony Brook University

Syllabus

1. Course Staff and Office Hours

Instructor: Peter Milder
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Light Eng. 231
Office Hours: TBD

Office hours may change. Please check Blackboard for up-to-date information.

2. Introduction

The field of digital system design has entered a new and complicated era. Digital designers now have increasingly large amounts of chip area to exploit, but they are strictly limited by the amount of power that can be consumed per transistor (the so-called "power wall"). Modern design practices must carefully balance a variety of system tradeoffs such as power, energy, area, throughput, latency, bandwidth, and reusability/customization of digital systems. This course will study how new design abstractions, languages, and tools can help address these problems from the system designer's perspective.

3. Course Description

Content of the course will fall into roughly three categories:

1. **Hardware Design Abstractions, Languages, and Tools:** register-transfer level design, simulation, and verification with the SystemVerilog hardware description language; parameterized "chip generator" tools; high-level synthesis (compilation of hardware from a high-level language); design-space exploration; domain-specific languages and tools.

2. **Limitations and Constraints of Modern Digital Systems:** the driving forces and limiting factors in current and near-future digital systems (the "power wall" and "utilization wall"); how these factors affect design practices and lead to a higher level of application-specific customization.

3. **New Architectures and Paradigms:** the evolution of field-programmable gate arrays; coarse-grained reconfigurable architectures; heterogeneous and hybrid computer systems.

4. Course Catalog Description

This course focuses on languages, tools, and abstractions for design and implementation of digital systems. Course material is divided roughly into three categories: Limitations and constraints on modern digital systems; Hardware design abstractions, languages, and tools (including the SystemVerilog hardware description language); and new architectures and paradigms for digital design. Coursework will be primarily project based; there will also be reading and discussion of published papers in these areas. Students should have experience with hardware description languages (VHDL, Verilog, or SystemVerilog) and software (C, C++ or Java).
Fall, 3 credits, grading ABCF.

5. Readings

Readings for this course will be in the form of research papers, which will be distributed in class or online.

Optional reference: "SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling," Stuart Sutherland, Simon Davidmann, and Peter Flake. Springer. Paperback (2010, ISBN 978-1441941251) or Hardcover (2006, ISBN 978-0387333991).

6. Grading

Grades will be based on attendance and participation, assignments, a final examination, and projects.

Assignments and participation	15%
Final examination	35%
Projects	50%

7. Academic Honesty

Academic honesty is very important. Only put your name on your own work. Written assignments must be completed in your own words; do not copy from other sources. For example, if you are assigned to read a research paper and answer questions about it, you may not copy text from that paper.

For projects, you may not share code outside of your group. You may not copy code or show your code to your classmates. Any copying or sharing of work or code will result in the assignment being scored a zero for all parties involved, with no exceptions. For group projects, if any member of the group commits academic dishonesty, the entire group will be equally penalized. All code will be automatically analyzed by a plagiarism detection tool.

For the final examination, any academic dishonesty will result in failing the course.

8. Piazza: Online Discussion Forum

This term we will be using Piazza for class discussion. The system is highly catered to getting you help fast and efficiently from classmates, the TAs, and myself. Rather than emailing questions to the teaching staff, I encourage you to post your questions on Piazza.

9. Schedule

Classes will be held in Frey Hall 205, from 4:00pm to 5:20pm on Mondays and Wednesdays.

The final examination will be held on Wednesday December 11, from 8:30pm to 11:00pm.

A full schedule with topics, assignments, and due dates will be available on Blackboard.

10. Student Learning Objectives

Students will acquire:

1. an ability to apply knowledge of mathematics, science, and engineering;
2. an ability to identify, formulate, and solve engineering problems;
3. an ability to communicate effectively; and
4. an ability to understand current research issues.

11. Electronic Communication Statement

Email and especially email sent via Blackboard (http://blackboard.stonybrook.edu) is one of the ways the faculty officially communicates with you for this course. It is your responsibility to make sure that you read your email in your official University email account. For most students that is Google Apps for Education (http://www.stonybrook.edu/mycloud), but you may verify your official Electronic Post Office (EPO) address at http://it.stonybrook.edu/help/kb/checking-or-changing-your-mail-forwarding-address-in-the-epo.

If you choose to forward your official University email to another off-campus account, faculty are not responsible for any undeliverable messages to your alternative personal accounts. You can set up Google Mail forwarding using these DoIT-provided instructions found at http://it.stonybrook.edu/help/kb/setting-up-mail-forwarding-in-google-mail.

If you need technical assistance, please contact Client Support at (631) 632-9800 or supportteam@stonybrook.edu.

12. Disability

If you have a physical, psychological, medical or learning disability that may impact your course work, please contact Disability Support Services, 128 ECC Building (631) 632-6748. They will determine with you what accommodations are necessary and appropriate. All information and documentation is confidential.

Students who require assistance during emergency evacuation are encouraged to discuss their needs with their professors and Disability Support Services. For procedures and information go to the following web site: http://www.ehs.sunysb.edu and search Fire Safety and Evacuation and Disabilities.

13. Academic Integrity Statement

Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty are required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology & Management, Nursing, Social Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including categories of academic dishonesty, please refer to the academic judiciary website at http://www.stonybrook.edu/commcms/academic_integrity/index.html

14. Critical Incident Management Statement

Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of Judicial Affairs any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn. Faculty in the HSC Schools and the School of Medicine are required to follow their school-specific procedures.