ESE 545 Computer Architecture Spring 2021

Course Description: This course focuses on the techniques of quantitative analysis and evaluation of modern computer systems. The emphasis is on instruction set design, pipelining, different types of parallelism (instruction, data, and thread level), and memory hierarchies. Students will undertake a design project on the multimedia processor design related to the course contents. The project is to be done with a use of hardware description languages, such as VHDL or Verilog/SystemVerilog, as well as modern CAD systems, such as Cadence, Mentor Graphics, etc.

Neither VHDL/Verilog languages nor the use of CAD systems will be taught in the class. Students are strongly encouraged to begin learning these tools individually starting from the first week of the class.

Instructor: Mikhail Dorojevets
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Course website: http://www.ece.stonybrook.edu/~midor/ESE545/index.html

Lectures: Thursday 6:30 - 9:20 PM **by Skype**
Office: 243 Light Engineering, 632-8611

Office hours: Wednesday 10:00 am - 12:00 pm **by Skype** (students need to request a time slot in advance)

Text: J. Hennessy and D. Patterson, Computer Architecture: A Quantitative Approach**, Sixth edition,** Morgan Kaufmann Publishers (Elsevier), 2019
ISBN: 978-0-12-811905-1

Other Highly Recommended Books:

1. Peter J. Ashenden. The Designer's Guide to VHDL, 2nd edition, Morgan Kaufmann Publishers, 2002. ISBN: 1-55860-674-2.

Exam: There will be one ("late mid-term") exam in April **by email**.
Project presentation deadline: Tuesday, **11:00 AM May 4 by email** to Instructor

Grading:

Exam:	50%
Project (one or two person teams):	50%