ESE 345

Computer Architecture

1. Course Staff and Office Hours

Instructor: Mikhail Dorojevets
Mikhail.Dorojevets@stonybrook.edu
243 Light Engineering

Office Hours: online by Skype on Monday, 10:00 –11:30 AM (when requested)
Other hours by appointment

TAs: Ryan Thielke (course subjects and **projects**)
Email: ryan.thielke@stonybrook.edu
TA hours:Tuesday 7:00-8:00 pm by Skype

Xiaokun Zhao (course subjects and **homeworks**)
Email: xiaokun.zhao@stonybrook.edu
TA hours: Friday 4:30-6:00 pm by Skype

Office hours may change. Please check the course website http://www.ece.stonybrook.edu/~midor/ESE345/index.html *for most up-to-date information.*

2. Course Description

This course focuses on the fundamental techniques of designing and evaluating modern computer architectures and tradeoffs present at the hardware/software boundary. The emphasis is on instruction set design, processor design, memory and parallel processing. Students will undertake a design project using a hardware description language and modern CAD tools.

Prerequisites: ESE 280 and ESE 382

Credits: 3

3. Textbook

David A. Patterson and John L. Hennessy “Computer Organization & Design The Hardware/Software Interface,” Fifth Edition by David A. Patterson and John L. Hennessy, 2014 by Elsevier Inc. ISBN:978-0-12-407726-3

4. Course Learning Objectives

To give students in-depth understanding of modern digital computer systems and tradeoffs present at the hardware-software interface. Based on that knowledge, they will be able to design principal processor components by applying the following design steps: definition of an instruction set architecture, cost/performance trade-offs, and gate-level and VHDL/Verilog design and implementation with modern CAD tools.

5. Student Learning Outcomes

Upon completion of this course, students will learn: 1) computer performance and instruction set design principles, 2) MIPS architecture and basics of assembly language programming, 3) integer and floating-point arithmetic, 4) processor, caches, and memory design, and 5) use of VHDL/Verilog languages in the processor datapath design and verification.

	Student Outcomes	% contribution
1	an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.	70
2	an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.	30
3	an ability to communicate effectively with a range of audiences.	
4	an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgements, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts.	
5	an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives.	
6	an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgement to draw conclusions.	

7	an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.	

6. Schedule

The updated course has not been offered yet but lectures will be held twice a week for 1 hour and 20 minutes each.

Week 1.	Introduction, technology overview, history of digital computers, instruction set architectures
Week 2.	Computer performance, and introduction to the MIPS architecture
Week 3.	MIPS operations and assembly-language programming
Week 4.	Adders, multipliers, dividers, and shifters
Week 5.	Floating point arithmetic: add and multiply.
Week 6.	*Midterm 1.* Design process, register transfer, single cycle datapath and control
Week 7.	Multiple cycle processor and multicycle controller
Week 8.	Pipelining
Week 9.	Pipelined processor datapath and control
Week 10.	Introduction to memory systems and SRAM/DRAM technology
Week 11.	Cache design
Week 12.	Virtual memory, translation look-aside buffers, and input/output basics
Week 13.	Review of multithreaded and multimedia processors. *Project presentations*.

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7. Assignments

7.1. Homework Assignments

Homework Assignments will be issued roughly weekly. A full schedule will be available on Blackboard. (This schedule will be updated as needed.) All assignments will be due at the *beginning* of class on the assigned day. Please see the Late Homework Policy, below.

All homework assignments must be submitted to **TA Xiaokun Zhao by email**.

7.2. Project

The project is **due on Nov. 30, 2020**. It must be submitted to **Instructor and TA Ryan Thielke by email**.

7.3. Collaboration Policy

Homework assignments are to be completed individually. You may *discuss* them with your classmates. However, you must write up your own solution individually without any help from any other person.

For example, it is fine if you and a friend discuss a problem together, and then separately work out the details and write your own separate solutions. On the other hand, it is not acceptable to share written solutions with another person or to create the written solutions together. In other words, the work you turn in must entirely be your own personal effort.

If you discuss homework problems with another person in the class, you must write "I discussed this assignment with…" and include the name(s) at the top of the assignment.

8. Grading

Your grade will be based on homework assignments, two midterm exams, and a project.

Homework Assignments	12%
Midterm Exam 1	33%
Midterm Exam 2	33%
Project	22%

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9. Academic Honesty

Any academic dishonesty on a written homework or lab will result in a zero grade for the assignment for all parties involved.

All exam work must be entirely your own with no collaboration or outside materials/information. Any academic dishonesty on the midterm exams or the project will result in failing the course. The case will be submitted to the College of Engineering's Committee on Academic Standing and Appeals.

10. Electronic Communication Statement

Email and especially email sent via Blackboard (http://blackboard.stonybrook.edu) is one of the ways the faculty officially communicates with you for this course. It is your responsibility to make sure that you read your email in your official University email account. For most students that is Google Apps for Education(http://www.stonybrook.edu/mycloud), but you may verify your official Electronic Post Office (EPO) address at http://it.stonybrook.edu/help/kb/checking-or-changing-your-mail-forwarding-address-in-the-epo.

If you choose to forward your official University email to another off-campus account, faculty are not responsible for any undeliverable messages to your alternative personal accounts. You can set up Google Mail forwarding using these DoIT-provided instructions found at http://it.stonybrook.edu/help/kb/setting-up-mail-forwarding-in-google-mail.

If you need technical assistance, please contact Client Support at (631) 632-9800 or supportteam@stonybrook.edu.
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11. Student Accessibility Support Statement

If you have a physical, psychological, medical, or learning disability that may impact your course work, please contact the Student Accessibility Support Center, 128 ECC Building, (631) 632-6748, or at sasc@Stonybrook.edu. They will determine with you what accommodations are necessary and appropriate. All information and documentation is confidential.

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12. Academic Integrity Statement

Each student must pursue their academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty is required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology & Management, Nursing, Social Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including categories of academic dishonesty please refer to the academic judiciary website at http://www.stonybrook.edu/commcms/academic_integrity/index.html

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13. Critical Incident Management Statement

Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of University Community Standards any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn. Faculty in the HSC Schools and the School of Medicine are required to follow their school-specific procedures. Further information about most academic matters can be found in the Undergraduate Bulletin, the Undergraduate Class Schedule, and the Faculty-Employee Handbook.